

## WHAT IS CLAIMED IS:

1           1.    An apparatus for controlling a physical layer interface  
2 of a network interface card, said apparatus comprising:

3               a read only memory (ROM) capable of storing an embedded  
4 control program;

5               a random access memory capable of storing a downloadable  
6 software control program; and

7               a microcontroller capable of controlling said physical  
8 layer interface, wherein said microcontroller in a first operating  
9 mode executes said embedded control program to thereby control said  
10 physical layer interface, and wherein said microcontroller in a  
11 second operating mode is capable of downloading said downloadable  
12 software control program from an external processing system and  
13 executing said software control program in place of said embedded  
14 control program to thereby control said physical layer interface.

1           2.    The apparatus as set forth in Claim 1 wherein said ROM is  
2 an internal ROM in said microcontroller.

1           3.    The apparatus as set forth in Claim 1 wherein said RAM is  
2 an internal RAM in said microcontroller.

1           4.    The apparatus as set forth in Claim 1 wherein said ROM is  
2   an external ROM coupled to said microcontroller.

1           5.    The apparatus as set forth in Claim 1 wherein said RAM is  
2   an external RAM coupled to said microcontroller.

1           6.    The apparatus as set forth in Claim 1 wherein said  
2   microcontroller downloads said downloadable software control  
3   program from said external processing system via a media  
4   independent clock (MDC) signal line and a media independent  
5   input/output (MDIO) signal line.

1           7.    The apparatus as set forth in Claim 6 wherein said  
2   microcontroller downloads said downloadable software control  
3   program via a medium access control (MAC) layer interface coupling  
4   said external processing system and said physical layer interface.

1           8.    The apparatus as set forth in Claim 1 wherein said  
2 microcontroller further comprises a plurality of control registers  
3 capable of controlling said first and second operating modes,  
4 wherein said microcontroller switches from said first operating  
5 mode to said second operating mode when said external processing  
6 system stores a jump address in said RAM in a first one of said  
7 plurality of control registers.

1           9.    A processing system comprising:

2               a data processor;

3               a hard disk drive capable of storing thereon a network  
4 interface card (NIC) configuration file containing a downloadable  
5 software control program; and

6               a network interface card for coupling said processing  
7 system to a data network, said network interface card comprising:

8               an apparatus for controlling a physical layer  
9 interface of said network interface card, said apparatus  
10 comprising:

11               a read only memory (ROM) capable of storing an  
12 embedded control program;

13               a random access memory capable of storing a  
14 downloadable software control program; and

15               a microcontroller capable of controlling said  
16 physical layer interface, wherein said microcontroller in  
17 a first operating mode executes said embedded control  
18 program to thereby control said physical layer interface,  
19 and wherein said microcontroller in a second operating  
20 mode is capable of downloading said downloadable software  
21 control program from an external processing system and  
22 executing said software control program in place of said

23 embedded control program to thereby control said physical  
24 layer interface.

1 10. The processing system as set forth in Claim 9 wherein  
2 said ROM is an internal ROM in said microcontroller.

1 11. The processing system as set forth in Claim 9 wherein  
2 said RAM is an internal RAM in said microcontroller.

1 12. The processing system as set forth in Claim 9 wherein  
2 said ROM is an external ROM coupled to said microcontroller.

1 13. The processing system as set forth in Claim 9 wherein  
2 said RAM is an external RAM coupled to said microcontroller.

1 14. The processing system as set forth in Claim 9 wherein  
2 said microcontroller downloads said downloadable software control  
3 program from said external processing system via a media  
4 independent clock (MDC) signal line and a media independent  
5 input/output (MDIO) signal line.

1           15. The processing system as set forth in Claim 14 wherein  
2           said microcontroller downloads said downloadable software control  
3           program via a medium access control (MAC) layer interface coupling  
4           said external processing system and said physical layer interface.

1           16. The processing system as set forth in Claim 9 wherein  
2           said microcontroller further comprises a plurality of control  
3           registers capable of controlling said first and second operating  
4           modes, wherein said microcontroller switches from said first  
5           operating mode to said second operating mode when said external  
6           processing system stores a jump address in said RAM in a first one  
7           of said plurality of control registers.

1           17. For use in a network interface card having a physical  
2 layer interface controllable by a microcontroller embedded therein,  
3 a method of operating the microcontroller comprising the steps of:

4                 in a first operating mode, executing an embedded control  
5 program stored in a read only memory (ROM) coupled to the  
6 microcontroller to thereby control the physical layer interface;

7                 in a second operating mode, downloading a software  
8 control program from an external processing system and storing the  
9 software control program in a random access memory (RAM) coupled to  
10 the microcontroller and, in response to the step of downloading the  
11 software control program, executing the software control program in  
12 place of the embedded control program to thereby control the  
13 physical layer interface.

14           18. The method as set forth in Claim 17 wherein the ROM is an  
15 internal ROM in the microcontroller.

16           19. The method as set forth in Claim 17 wherein the RAM is an  
17 internal RAM in the microcontroller.

1           20. The method as set forth in Claim 17 wherein the ROM is an  
2 external ROM coupled to the microcontroller.

1           21. The method as set forth in Claim 17 wherein the RAM is an  
2 external RAM coupled to the microcontroller.

1           22. The method as set forth in Claim 17 wherein the step of  
2 downloading comprises the step of downloading the software control  
3 program from the external processing system via a media independent  
4 clock (MDC) signal line and a media independent input/output (MDIO)  
5 signal line.

1           23. The method as set forth in Claim 22 wherein the step of  
2 downloading comprises the step of downloading the software control  
3 program via a medium access control (MAC) layer interface coupling  
4 the external processing system and the physical layer interface.